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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Martin Ceredig Roberts et al. Examiner: Unknown
Serial No.: Unknown Group Art Unit: Unknown

Filed: Herewith Docket: 303.451US6

Title: METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT

**USING A DUAL POLY PROCESS** 

## PRELIMINARY AMENDMENT

Box Patent Application Commissioner for Patents Washington, D.C. 20231

Before taking up the above identified application for examination, please enter the following amendments.

## IN THE SPECIFICATION

On page 1, after the title, please insert, - This application is a Continuation of U.S. Application No. 09/351,884, filed July 13, 1999, which is a Continuation of Application No. 08/390,714, filed February 17, 1995.--

## IN THE CLAIMS

Please cancel claims 1-33 after adding the following new claims:

34. (New) A semiconductor interconnect, comprising:

a substrate layer having a first substrate region and a second substrate region;

a first silicon plug in electrical contact with the first substrate region and extending vertically above the substrate layer;

a second silicon plug in electrical contact with the second substrate region and extending vertically above the substrate layer;

an oxide layer overlaying the substrate layer and located between the first and second silicon plugs; and

a first silicon layer capable of electrical conduction overlaying the oxide layer and interposed between the first and second silicon plugs, the first silicon layer has only vertical interfaces with the first and the second silicon plugs.

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